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NASA CASE NO. MFS-28458-1

PRINT FIG. #1

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(NASA-Case-MFS-28458-1) CONTROL CIRCUITRY USING ELECTRONIC EMULATION OF A SYNCHRO SIGNAL FOR ACCURATE CONTROL OF POSITION AND RATE OF ROTATING SHAFTS Patent Application (NASA) 16 p
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CSCL 09A G3/33
Unclas
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CONTROL CIRCUITRY USING ELECTRONIC EMULATION OF A SYNCHRO SIGNAL FOR ACCURATE CONTROL OF POSITION AND RATE OF ROTATION FOR SHAFTS

Patent Application Abstract

NASA Case MFS-28458

The present invention is broadly related to servomechanisms and control systems for accurate control of rotating shaft position and rate of rotation. More specifically, this invention is related to feedback control systems which typically include a synchro, a drive motor for the synchro with associated rate control, a resolver and a controlled motor which drives the rotating shaft to be controlled.

The subject invention replaces the synchro, drive motor and associated rate control elements in a synchro-resolver follower system with a digital and analog synchro emulation circuit for generating the resolver control signal.

The synchro emulation circuit includes amplitude modulation means to provide relatively high frequency resolver excitation signals for accurate resolver response even with very low shaft rotation rates.

As illustrated in FIGS. 1 and 2, the synchro emulation circuit 1 includes a clock oscillator 10 which controls the operation of a counter 20. The output of the counter 20 is used for addressing a pair of read only memories 22 and 24. The first read only memory 22 contains digitized sine information and the second read only memory 24 contains digitized cosine information. As the counter 20 increments or decrements, information is passed from the read only memories 22 and 24 to a corresponding pair of digital to analog

converters 26 and 28 which in turn provide corresponding analog sine and cosine wave outputs. These waveforms are each multiplied or modulated with a carrier frequency and then used as an excitation signal for a corresponding resolver stator input. A multiplexer circuit 14 is employed between the oscillator 10 and the counter 20 to enable the counter frequency to be chosen from a plurality of frequencies so as to allow a desired rotational rate to be selected for the shaft under control.

The present invention can be used in the synchronization of two or more shafts which are rotating at extremely low rates.

In the present invention, the low frequency sine and cosine waves are multiplied with a high frequency carrier signal and the resulting modulated signals are applied to the respective stator inputs. The signal generated by the resolver rotor is then coherently demodulated to obtain an error signal which is used to control a power amplifier to drive the controlled motor.

It appears that the novelty of the present invention lies in the circuit configuration used to realize the emulation of a synchro device. It appears that this invention may find very broad use in the conduct of aeronautical and space activities as this may be used as part of a control system to control accurately both position and rate of rotation for a plurality of shafts.

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Serial Number:	07/710192

PATENT
MFS-28458-1

Serial No. 07/710192
Filing Date June 3, 1991

CONTROL CIRCUITRY USING ELECTRONIC EMULATION OF A SYNCHRO SIGNAL FOR ACCURATE CONTROL OF POSITION AND RATE OF ROTATION FOR SHAFTS

Origin of the Invention

The invention described herein was made by employees of the United States Government and may be manufactured and used by or for the Government for Government purposes without the payment of any royalties thereon or therefore.

Technical Field

The present invention is broadly related to servo mechanisms and control systems for accurate control of rotating shaft position and rate of rotation. More specifically, this invention is related to feedback control systems which typically include a synchro, a resolver and a controlled motor. The invention disclosed herein is directed particularly to a digital circuit which emulates a synchro signal in a synchro-resolver follower system.

Background Art

Synchro-resolver systems or devices are typically employed to sense and control the position of rotating shafts accurately. In older prior art synchro-resolver systems, a motor is employed to drive a synchro at a particular rate or rotational velocity. The synchro produces a control signal which is fed into a resolver. The output of the resolver is then fed to a demodulator which produces an error signal that is input to an amplifier which drives the motor to be controlled.

The disadvantages of the previous methods are the cost, weight and corresponding electrical and mechanical hardware requirements for the additional drive motor and synchro. In addition, conventional resolver shaft position controlling circuits cannot be employed at very low speeds because the resolver must be excited by sine and cosine waveforms of fairly high frequency in order to function properly.

There have been attempts to overcome the limitations of conventional electro-mechanical synchros with the substitution of analog circuit synchro signal generators. An analog emulation of this synchro signal is undesirable, however, due to the instabilities of signals produced in analog circuitry.

Other prior art resolver excitation circuits have included digital circuit elements. For example, U.S. patent 4,204,257 discloses a resolver position measuring device which includes a digital counter, a pair of read only memory means for providing sine and cosine sequences and a pair of digital to analog converters to generate sine and cosine analog waveforms for resolver excitation. Circuits such as this do not solve the problem of poor resolver low frequency response.

Disclosure of Invention

The object of the present invention is to provide a digital and analog control circuit, for generating modulated analog resolver excitation signals and recovering an error signal from a resolver, having the advantageous circuit topology herein disclosed.

The subject invention replaces the synchro and drive motor with a synchro emulation circuit for generating the resolver excitation signal. The synchro emulation circuit includes a clock oscillator which controls the operation of a counter. The output of the counter is used for addressing a pair of read only memories (ROMs), a first ROM which contains digitized sine information and a second ROM which contains digitized cosine information. As the counter increments or decrements, information is passed from the ROMs to a corresponding pair of digital to analog (D/A) converters which in turn provide corresponding analog cosine and sine wave outputs. These waveforms are each multiplied with a carrier frequency and then used as an excitation signal for a corresponding resolver stator input.

A frequency divider and multiplexer circuit is employed between the crystal clock oscillator and the counter to enable the counter frequency to be chosen from a plurality of frequencies to allow a desired rotational rate to be selected.

The present invention solves the problem of poor resolver low frequency response by multiplying the low frequency sine and cosine waves with a high frequency carrier signal and then applying the resulting modulated signals to the respective resolver stator inputs. The signal generated by the resolver rotor is then demodulated to obtain an error signal which is input to a power amplifier for a controlled motor, to maintain the shaft at a desired rotational velocity and position. By employing a plurality of these resolver circuits, all controlled by the same oscillator, the speeds and relative positions of a plurality of shafts can be accurately controlled.

Brief Description of the Drawings

The objects, features, and advantages of the present invention will become apparent from a consideration of the following detailed description of a preferred embodiment thereof, taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a circuit that forms a preferred embodiment of the subject invention; and,

FIG. 2 is a schematic diagram of a portion of the circuit illustrated in FIG. 1.

Best Mode for Carrying Out the Invention

Turning now to a more detailed consideration of a preferred embodiment of the present invention, there is illustrated in FIGs. 1 and 2, a synchro emulation circuit 1 including a single crystal clock oscillator 10 which provides a periodic signal to a frequency divider 12. In the preferred embodiment, the crystal clock oscillator provides a 4.194304 Megahertz (MHz) signal which is divided down to a 4.096 kilohertz (KHz) carrier signal. The 4.096 KHz signal is conditioned to provide a stable -10 volt to +10 volt output. In the preferred embodiment, the frequency divider 12 is capable of providing 8 separate frequencies in output, they are: 256 Hz, 512 Hz, 1024 Hz, 2048 Hz, 4096 Hz, 8192 Hz, 16384 Hz and 32768 Hz.

The output of the frequency divider 12 is input to a multiplexer 14 and signal conditioning circuitry 16. The 8 to 1 multiplexer chooses one of the 8 frequencies available on the frequency divider in response to control signals from a trio of multiplexer control lines 18. The signal conditioning circuitry 16 provides a conditioned 4.096 KHz output signal as a carrier signal.

The multiplexer provides a selected frequency as an input to counter 20. The counter output may optionally either increment or decrement in response to a counter control signal on the counter control line 22. The counter may also be stopped at a given count by the addition of an optional switched clock control line 24. Counter functions such as increment, decrement and stop are not shown in the embodiment of FIG. 2, but these functions are easily added with currently available integrated circuits. The output from the counter is provided as an input to a sine information ROM 26 and a cosine information ROM 28. The output from the sine information ROM is provided as an input to a first D/A converter 30. The output of the cosine information ROM is provided as an input to a second D/A converter 32.

The analog output from the first D/A converter 30 is a sine wave which is fed into a first analog multiplier 34. A second input to the first analog multiplier 34 is the conditioned carrier signal output from the signal conditioning circuitry 16. The first analog multiplier 34 multiplies the analog sine wave output from the first D/A converter and the 4.096 KHz carrier signal to provide a first output signal to a resolver 36, or to an equivalent position sensing device. The first multiplier output signal to the resolver input is:

sine (carrier) * sine (selected frequency)

The "sine (carrier)" term in this expression represents a conditioned carrier which can be a sine wave or any other periodic signal. In one embodiment a square wave is the carrier, however the carrier could be a triangular wave or a sawtooth wave.

The output of the second D/A converter 32 is a cosine wave which is provided as an input to a second analog multiplier 38. The second analog multiplier 38 has as a second input the 4.096 KHz conditioned output of the signal conditioning circuit 16. The analog multiplier multiplies the cosine waveform and the conditioned carrier signal to generate the second resolver input signal, which is:

sine (carrier) * cosine (selected frequency)

As mentioned above the "sine (carrier)" term may be a sine wave, a square wave, a triangular wave or a sawtooth wave. The only limitation is that the carrier must be a periodic waveform. The second resolver input must use the same conditioned carrier signal as the first resolver input, i.e. a square wave conditioned carrier signal may be used for both multiplier inputs. For this implementation, the selected shaft rotation frequencies can be:

1/16 Hz, 1/8 Hz, 1/4 Hz, 1/2 Hz, 1 Hz, 2 Hz, 4 Hz and 8 Hz.

A demodulation circuit 40 receives an input signal from the resolver 36, or from the equivalent sensing device. The demodulation circuit 40 combines this input with the output of the signal conditioning circuit 16 for coherent amplitude demodulation of the error signal. The demodulation circuit 40 produces an error signal which is then provided as an input to a compensation circuit 42. The compensated output signal from the compensation circuit 42 is an input to a power amplifier 44 for a controlled motor.

As illustrated in FIG. 2, the various circuit elements of the synchro emulation circuit 1 can be chosen as indicated by the following table:

ELEMENT NUMBER	IC IDENTIFICATION NUMBER
12	MM74HC4020
14	MM74HC4051
16	741 OP AMP and associated circuit elements
20	MM74HC4040
26, 28	NMC27C32
30, 32	MN370
34, 38	MPY 100G
40	741 OP AMP and associated circuit elements

Turning now to operational details, the 4.194304 MHz clock 10 provides an input to the divider 12 and multiplexer 14 which gives 8 selectable outputs of binary multiples from 256 Hz through 32768 Hz. The divider 12 also provides the 4096 Hz carrier signal.

As shown in FIG. 2, the MM74HC4020 divider 12 provides the 4096 Hz signal in a 0-5 volt waveform. Conditioning circuit 16 converts this to a -10V to +10V conditioned carrier signal.

The selectable frequencies are used to vary the rotational rate of the motor being controlled. The selected frequency is input to the 12 bit counter 20. The output of this counter is used for addressing the sine ROM 26 and the cosine ROM 28. The sine ROM contains digitized sine information and the cosine ROM contains digitized cosine information. As the counter 20 increments (or, for another counter, not the 74HC4040, decrements), information is passed from each of the ROMs to first and second D/A converters 30 and 32, respectively. The outputs from the D/A converters are a sine waveform and a cosine waveform, each oscillating at a frequency corresponding to the desired shaft rotational rate

The sine and cosine waves are each multiplied with (or amplitude modulated by) the carrier frequency in the analog multiplier circuits 34 and 38. These multiplied signals are used as excitation signals for the resolver 36. These signals are similar to what would be provided by a synchro in a standard synchro-resolver follower application. However, since the excitation signals are amplitude modulated up into the kilohertz frequency range, problems with resolver low frequency response are avoided and a typical resolver may be employed for applications in which very slow shaft rotation rates are desired. The excitation signals, modulated in this way, contain both position and rate of rotation commands. When the first and second stator inputs of the resolver 36 are excited with these modulated signals, the resolver stator output signal needs only to be demodulated to generate a true error signal. The purpose of the resolver 36 is to convert the excitation signals into an error signal.

The output of the resolver 36 is demodulated from the carrier frequency in the demodulation circuit 40 to provide the error signal used in controlling the motor. FIG. 2 shows a simple circuit for coherent amplitude demodulation as is well known in the art. The error signal is the difference between the desired rotational position and the actual rotational position of the motor.

The disclosed embodiment should not be interpreted as limiting the present invention. There are a number of alternate embodiments which could be realized within the scope and spirit of the invention. For example, the frequency of the crystal controlled oscillator can be adjustable or the oscillator can be replaced with a voltage controlled oscillator, to give a wider dynamic range for commanded rotational rates. In addition, a stationary position of the motor can easily be realized by withholding or stopping the clock to the counter at a count corresponding to the desired angular position. In addition, increased accuracy and resolution for this controller could be realized by increasing the size of the ROM storage means, thereby allowing enhanced resolution of the digitized sine and cosine information. The present embodiment could also be altered to provide increased accuracy by utilizing higher resolution D/A converters. Any such modification simply requires the number of data lines from the ROM means to be equal to the number of input lines for the D/A converters. Finally, the direction of rotation could be selectable by replacing the 12 bit counter 20 with a 12 bit up/down counter and providing a means for controlling the counter.

Although the invention has been disclosed in terms of a preferred embodiment, it should be understood that numerous modifications and variations could be made thereto without departing from the true spirit and scope thereof as defined by the following claims.

Abstract of the Disclosure

The invention herein disclosed is a digital circuit which emulates a synchro signal in a synchro-resolver follower system for precise control of shaft position and rotation at very low rotational rates. The subject invention replaces the synchro and drive motor in a synchro-resolver follower system with a digital and analog synchro emulation circuit for generating the resolver control signal. The synchro emulation circuit includes amplitude modulation means to provide relatively high frequency resolver excitation signals for accurate resolver response even with very low shaft rotation rates.

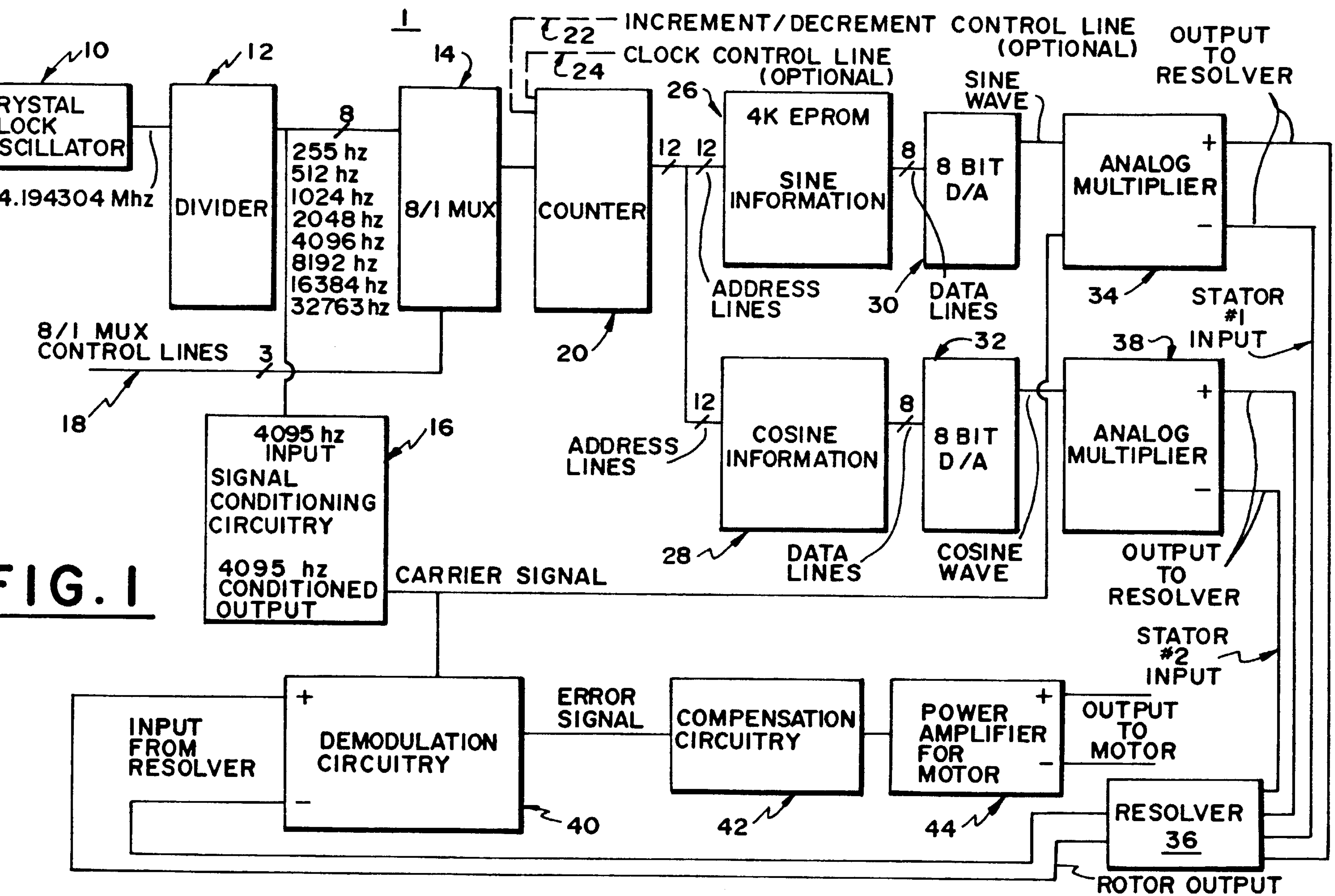
1
RYSTAL
LOCK
SCILLATOR
10
4.194304 Mhz
DIVIDER
12
8
255 hz
512 hz
1024 hz
2048 hz
4096 hz
8192 hz
16384 hz
32763 hz
8/1 MUX
14
8/1 MUX
CONTROL LINES
3
18
22
INCREMENT/DECREMENT CONTROL LINE
(OPTIONAL)
24
CLOCK CONTROL LINE
(OPTIONAL)
COUNTER
20
12
12
26
4K EPROM
SINE
INFORMATION
ADDRESS
LINES
8
30
DATA
LINES
8 BIT
D/A
SINE
WAVE
ANALOG
MULTIPLIER
34
OUTPUT
TO
RESOLVER
STATOR
#1
INPUT
4095 hz
INPUT
SIGNAL
CONDITIONING
CIRCUITRY
4095 hz
CONDITIONED
OUTPUT
16
ADDRESS
LINES
12
COSINE
INFORMATION
28
8
DATA
LINES
32
8 BIT
D/A
COSINE
WAVE
38
ANALOG
MULTIPLIER
OUTPUT
TO
RESOLVER
STATOR
#2
INPUT
CARRIER SIGNAL
INPUT
FROM
RESOLVER
DEMODULATION
CIRCUITRY
40
ERROR
SIGNAL
COMPENSATION
CIRCUITRY
42
POWER
AMPLIFIER
FOR
MOTOR
44
OUTPUT
TO
MOTOR
RESOLVER
36
ROTOR OUTPUT

FIG. I

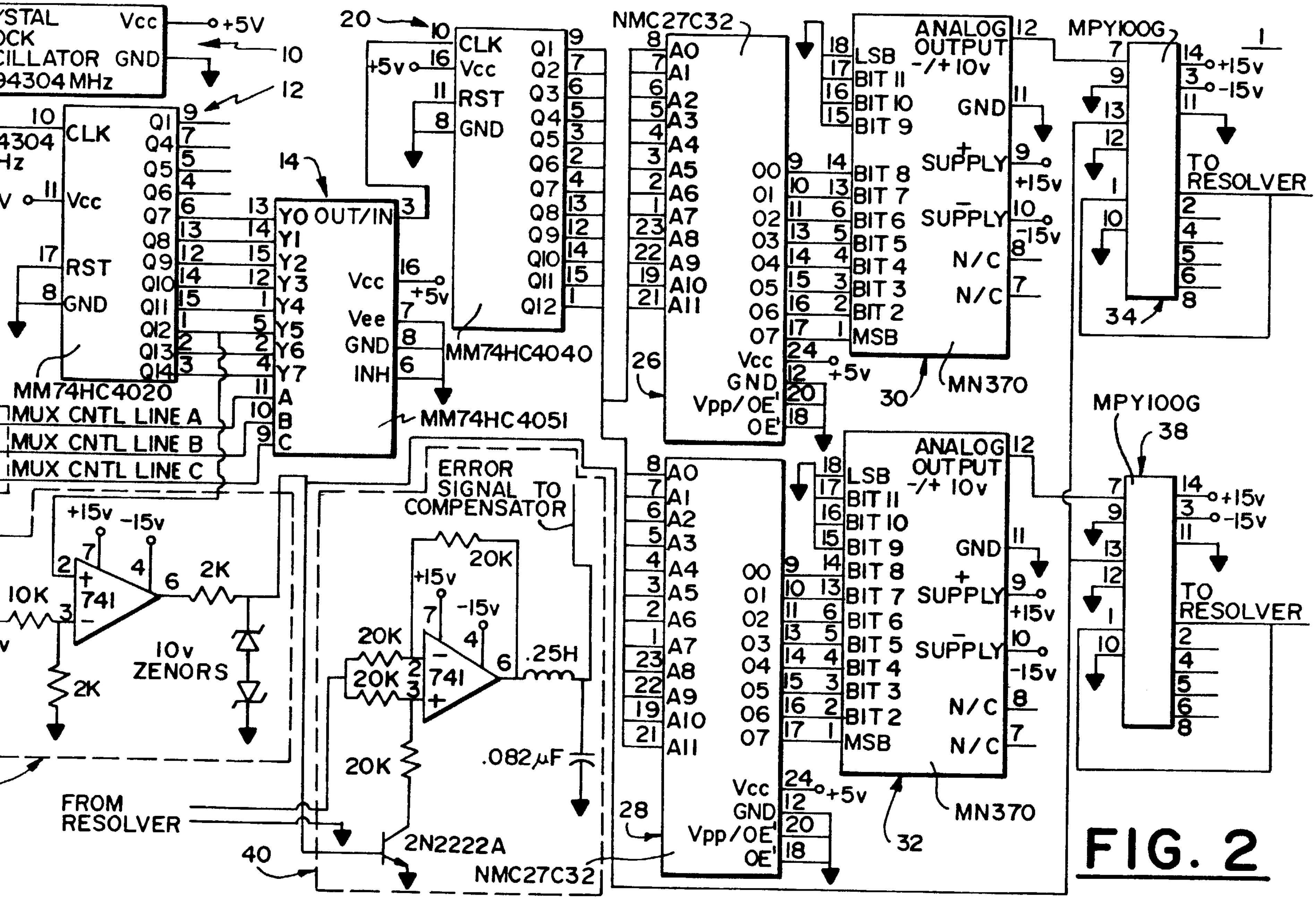
CRYSTAL CLOCK OSCILLATOR 4.194304 MHz
Vcc
GND
+5V
10
12
MM74HC4020
CLK
RST
GND
Q1 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14
MUX CNTL LINE A
MUX CNTL LINE B
MUX CNTL LINE C
14
MM74HC4051
Y0 OUT/IN
Y1 Y2 Y3 Y4 Y5 Y6 Y7
A B C
Vcc Vee GND INH
+5v
20
MM74HC4040
CLK Vcc RST GND
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12
NMC27C32
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
00 01 02 03 04 05 06 07
Vcc GND Vpp/OE' OE'
26
28
MN370
ANALOG OUTPUT -/+ 10v
LSB BIT 11 BIT 10 BIT 9 BIT 8 BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 MSB
GND
+ SUPPLY
− SUPPLY
N/C
+15v
-15v
30
32
MPY100G
34
38
TO RESOLVER
ERROR SIGNAL TO COMPENSATOR
741
10K
2K
20K
10v ZENORS
.25H
.082μF
2N2222A
FROM RESOLVER
40

FIG. 2